EEEN202 Lab 3 Sequential Logic: Counters

Section 3

3.1 – J-K FF

Initial state: Enable: 1, Reset: 0, Clear: 0, J = 1, K = 1, Q = 0

|  |  |  |  |
| --- | --- | --- | --- |
| J | K | Q after CLK pulse | Resulting FF |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

1. The FF transitions off LO to HI pulse i.e., it’s a rising edge FF
2. When enable goes LO, the FF stops operating. The current state of the FF persists
3. When Preset goes HI, nothing changes. If Reset goes HI whilst Preset = HI, the FF transitions to the set state, or FF = 1
4. When Clear/K goes HI, and Q = 1, FF transitions and Q = 0 and /Q = 1. If /Q = 1, then nothing changes

3.2 – 4 Bit asynchronous counter using rising edge J-K FF + 3.3 – Timing diagram

Graphical user interface

Description automatically generated

3.4 – Circuitverse and table

Diagram

Description automatically generated

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| CLK Pulse | D | C | B | A |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |
| 11 | 1 | 0 | 1 | 1 |
| 12 | 1 | 1 | 0 | 0 |
| 13 | 1 | 1 | 0 | 1 |
| 14 | 1 | 1 | 1 | 0 |
| 15 | 1 | 1 | 1 | 1 |
| 16 | 0 | 0 | 0 | 0 |
| 17 | 0 | 0 | 0 | 1 |

3.5

Diagram

Description automatically generated

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| CLK Pulse | D | C | B | A |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 |
| 2 | 1 | 1 | 0 | 1 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 1 | 0 | 1 | 1 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 1 | 0 | 0 | 1 |
| 7 | 1 | 0 | 0 | 0 |
| 8 | 0 | 1 | 1 | 1 |
| 9 | 0 | 1 | 1 | 0 |
| 10 | 0 | 1 | 0 | 1 |
| 11 | 0 | 1 | 0 | 0 |
| 12 | 0 | 0 | 1 | 1 |
| 13 | 0 | 0 | 1 | 0 |
| 14 | 0 | 0 | 0 | 1 |
| 15 | 0 | 0 | 0 | 0 |
| 16 | 1 | 1 | 1 | 1 |
| 17 | 1 | 1 | 1 | 0 |

3.6 – With each additional FF, the CLK frequency is halved. In this case, the output frequency:

Where (and n is the number of FFs used. With 4 FFs used, its MOD number is 16; for an input signal of 10 kHz, then the output frequency is 625 kHz.

3.7 – MOD 10 counter

Diagram

Description automatically generated

Section 4

4.1 – J-K edge-triggered flip-flop

|  |  |  |  |
| --- | --- | --- | --- |
| Inputs before nth CLK pulse | | Outputs after nth CLK pulse | |
| J | K |  |  |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

4.2

Set line (active low): when pulled to LO, Q of all the FF’s gets locked to HI i.e., pulsing the CLK of the first FF does nothing. Pulsing LO sets Q of all FF’s to HI, but does not lock it

Clear line (active low): when pulled to LO, Q of all the FF’s gets locked to LO. Pulsing LO sets Q of all the FF’s to LO.

4.3

(i) MOD 12 counter: NAND gate with inputs from D and C

(ii) MOD 10 counter: NAND gate with inputs from D and B

4.4

(i) Down counter: take the output or use a NOT gate for each output

(ii) Flexible counter: have an XOR gate for each output of an up counter. One input is the output of an FF and the other is tied to a switch. When turned on, the XOR turns into NOT gate, turning the up counter into a down counter. Circuitverse example:

Diagram

Description automatically generated

Section 5

5.(i) – 50hz to 1hz converter (Circuitverse sim)

MOD 50 counter using the reset AND gate as the output

Diagram

Description automatically generated